Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Currently Amended). A method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining if the initiator or the interconnect is to be responsible for ordering packet-format responses to packet-format requests issued by said initiator;

determining whether to define a maximum number of packet format requests which are permitted to be outstanding at the same time; [[and]]

defining if a delay stage is required in said initiator; and

wherein the initiator is usefully embodied in the integrated circuit.

2(Previously Presented). A method as claimed in claim 1, wherein said number of requests which are permitted to be outstanding are defined when the interconnect is responsible for ordering.

3(Previously Presented). A method for designing a target in an integrated circuit, said target being connected to an interconnect and arranged to generate packet format responses to packet format requests, the method comprising the steps of:

defining if the target or the interconnect is responsible for ordering responses;

determining whether to define a maximum number of possible outstanding requests which can be supported by said target; [[and]]

defining if a delay stage is required in said target; and

wherein the target is usefully embodied in the integrated circuit.

4(Previously Presented). A method as claimed in claim 3, wherein said step of defining the maximum number of possible outstanding requests is performed when the interconnect is responsible for ordering the responses.

5(Currently Amended). A method for designing an interconnect having routing resources, said interconnect arranged to allow initiators to send packet-format requests to targets, said method comprising the steps of defining:

the number of routing resources between the initiator and the target;

the arbitration method for arbitrating between requests; and

the association between the routing resources and the targets; and

wherein the interconnect is usefully embodied in an integrated circuit.

6(Original). A method as claimed in claim 5, wherein said method further comprises the step of determining if a delay is required after arbitration.

7(Currently Amended). A method for designing an interconnect having routing resources, said interconnect arranged to allow targets to send packet-format responses to initiators in response to packet-format requests from initiators, said method comprising the steps of defining:

the number of routing resources between the target and the initiator;

the arbitration method for arbitration between responses; [[and]]

the association between the routing resources and the initiator

wherein the interconnect having routing resources is usefully embodied in an integrated circuit.

8(Original). A method as claimed in claim 7, wherein said method further comprises the step of determining if a delay is required after arbitration.

9(Currently Amended). A method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model; and

wherein the arbiter is usefully embodied in an integrated circuit.

10(Currently Amended). A method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said initiators and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model, wherein the method further comprises selecting if a delay is to be provided after arbitration has been performed; and

wherein the arbiter is usefully embodied in an integrated circuit.

11(Currently Amended). A method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model; and

wherein the interconnect having routing resources is usefully embodied in an integrated circuit.

12(Currently Amended). A method of designing an arbiter in an integrated circuit comprising initiators and targets, and an interconnect coupled to communicate packets between the initiators and targets, said arbiter being provided between said targets and said interconnect, said method comprising the steps of:

using an arbitration model having a plurality of different arbitration methods, wherein each arbitration method specifies whether the initiator is responsible for ensuring time based ordering of packets is handled, and selecting one of the plurality of arbitration methods available in said model, wherein the method further comprises selecting if a delay is to be provided after arbitration has been performed; and

wherein the arbiter is usefully embodied in an integrated circuit.

13(Currently Amended). A model of an initiator to be used in designing an integrated circuit in which an initiator is arranged to send packet-format requests to one or more targets via an interconnect, said model embodied in a tangible media and said model comprising:

an address decode stage for identifying the target for which a given message is intended; and

a dependency stage for determining the allowability of a request, the operation of said dependency stage being selectable, said dependency stage being such that the model supports an arrangement where the initiator or the interconnect is responsible for maintaining the order of packet-format responses from a target to the requests.

14(Original). A model as claimed in claim 13, wherein a retime stage is provided in said model, the retime stage arranged to provide a delay or no delay.

15(Previously Presented). A model as claimed in claim 13, wherein an access queue is provided for storing requests for which responses have not been received.

16(Original). A model as claimed in claim 15, wherein the maximum number of requests which can be stored in the queue is definable.

17(Previously Presented). A model of a target to be used in designing an integrated circuit in which one or more initiators are arranged to send packet-format requests to a target and the target is arranged to send packet-format responses to the requests via an interconnect, said model embodied in a tangible media and said model comprising:

a locking stage which permits locked transactions to occur if required; and

a decode state which decodes information stored in a first queue into an address for the response.

18(Previously Presented). A model as claimed in claim 17, wherein said model comprises an access queue which stores information on the requests received by the target.

19(Previously Presented). A model as claimed in claim 18, wherein a maximum number of outstanding requests which can be stored in said first queue is definable.

20(Original). A model as claimed in claim 17, wherein said queue is in the initiator.

21-24 (Cancelled).

25(Previously Presented). A method for designing an initiator in an integrated circuit, said initiator being connected to an interconnect and arranged to issue packet-format requests, said method comprising the steps of:

defining if the initiator or the interconnect is to be responsible for ordering packet-format responses to requests issued by said initiator; and

defining if a delay stage is required in said initiator; and

wherein the initiator is usefully embodied in an integrated circuit.